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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,089	10/12/2001	G. Michael Uhler	MIPS:0140.00US	1887

23669 7590 05/25/2006

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,089	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-27 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-27 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050930*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Requirement for Information

1. Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the Examiner has determined is reasonably necessary to the examination of this application.

2. In response to this requirement, please provide a copy of each of the following items of art referred to in the Specification: Software User's Manual for the MIPS32 of MIPS64 Processor Core Family, Section 5 "CP0 Registers", pages 70-106 (See Page 18 Paragraph 0041).

3. The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

4. The Applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the Applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained may be accepted as a complete reply to the requirement for that item.

5. This requirement is an attachment of the enclosed Office action. A complete reply to the enclosed Office action must include a complete reply to this requirement. The time period for reply to this requirement coincides with the time period for reply to the enclosed Office action.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 10, 11, 12, 13, 14, 16, 17, 20, 21, 22, 23, 24, 27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" ("MCF5206") and Freescale Semiconductor, Inc.

"Addendum to MCF5206 User Manual" ("MCF5206 Addendum"), and US Patent Number 5,025,368 to Watenabe ("Watenabe").

8. In reference to Claim 10, MCF5206 discloses a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5), the microprocessor comprising: a core for executing instructions (See Page 1 Paragraph 3); and generating second interrupts by devices internal to the microprocessor (See 'Interrupt Controller' on Page 5). Because the interrupt priorities are programmable, MCF5206 will inherently include priority storage logic for storing the programmable priorities of the second interrupts (See 'Interrupt Controller' on Page 5). MCF5206 will inherently have a priority encoder coupled to the core for prioritizing the first and second interrupts utilizing the fixed priorities for the first interrupts and the programmable priorities for the second interrupts (See Page 2 'System Interface' – 'Programmable Interrupt Controller'). MCF5206 does not disclose that the second interrupts are generated by the core. Watanabe teaches a CPU core comprising segments commonly used to form a complete microprocessor, such as timers and I/O units (See Column 1 Lines 55-57 and Column 2 Lines 50-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the MCF5206 with the internal peripheral devices as part of the core, resulting in the invention of Claim 10, in order to allow it to be easily interfaced with various peripheral devices, to minimize the area needed by the

microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41-46; and Column 4 Lines 1-16 of Watanabe).

9. In reference to Claim 11, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 further discloses that the interrupt controller receives a plurality of third interrupts from sources thereof, prioritizes said third interrupts, and provides the prioritized third interrupts to the microprocessor as the first interrupts (See 'Interrupt Controller' on Page 5).

10. In reference to Claim 12, MCF5206 and Watanabe teach the limitations as applied to Claim 11 above. MCF5206 further discloses that the first interrupts are presented to the processor on first interrupt signal lines attached to the microprocessor (See Figure on Page 6).

11. In reference to Claim 13, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 Addendum discloses that the instructions executed by the core of the MCF5206 comprise: JSR, BSR, and RTS instructions, which are both instructions for handling the first interrupts and instructions for handling the second interrupts (See Pages 3-5). MCF5206 further discloses third instructions for storing said programmable priorities into said priority storage means (See 'Interrupt Controller' on Page 5).

12. In reference to Claim 14, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 further discloses that the plurality of first interrupts comprise timer interrupts, which are hardware interrupts (See 'Timer Module' on Page 4). MCF5206 Addendum discloses that the MCF5206 also includes a TRAP instruction, which is a software interrupt (See Page 5).

13. In reference to Claim 16, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 further discloses that that there are a plurality of internal interrupts that can each be programmed to a different priority (See 'Interrupt Controller' on Page 5), and thus the priority storage logic must inherently include a plurality of interrupt fields each corresponding to one of the second interrupts.

14. In reference to Claim 17, MCF5206 and Watanabe teach the limitations as applied to Claim 16 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities which require a minimum 5-bit field (which allows a maximum of 32 distinct values) to store. A 4-bit field is a subset of a 5-bit field, and thus a 4-bit field providing 16 distinct interrupt priorities is inherently a part of MCF5206.

15. In reference to Claim 20, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 further discloses that each external interrupt signal can be programmed to one of 3 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 12 distinct interrupt priorities. Eight distinct interrupt priorities is a subset of a 12 distinct interrupt priorities, and thus 8 distinct interrupt priorities for the first interrupts is inherently a part of MCF5206.

16. In reference to Claim 21, MCF5206 and Watanabe teach the limitations as applied to Claim 20 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities. The 28 internal interrupt levels overlap with the 12 external interrupt levels (See 'Interrupt Controller' on Page 5).

17. In reference to Claim 22, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. MCF5206 further discloses that that the priority encoder, when prioritizing the first and second interrupts, also uses priorities for the first interrupts established by the interrupt controller (See 'Interrupt Controller' on Page 5).

18. In reference to Claim 23, MCF5206 and Watanabe teach the limitations as applied to Claim 10 above. The priority encoder of MCF5206 will inherently produce an indication of which of the first and second plurality of interrupts has the highest priority.

19. In reference to Claim 24, MCF5206 and Watanabe teach the limitations as applied to Claim 23 above. MCF5206 further discloses a vector generator for producing an interrupt vector corresponding to the interrupt having the highest priority (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

20. In reference to Claim 27, MCF5206 and Watanabe teach a method for prioritizing on-core and off-core interrupts in a processing system, comprising: receiving the off-core interrupts, the off-core interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5); receiving the on-core interrupts, the on-core interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts (See 'Interrupt Controller' on Page 5). MCF5206 will inherently prioritize the on-core and off-core interrupts according to their priority levels produce an indication of which of the first and second plurality of interrupts has the highest priority.

21. In reference to Claim 29, MCF5206 and Watanabe teach the limitations as applied to Claim 27 above. MCF5206 further discloses that the off-core interrupts are initially prioritized by an interrupt controller (See 'Interrupt Controller' on Page 5).

22. In reference to Claim 30, MCF5206 and Watanabe teach the limitations as applied to Claim 27 above. MCF5206 will inherently select the received internal or off-

core interrupt with the highest priority level by examining the priority levels of each of the received internal and off-core interrupts (See 'Interrupt Controller' on Page 5).

Specification

23. The attempt to incorporate subject matter into this application by reference to "Software User's Manual for the MIPS32 of MIPS64 Processor Core Family, Section 5 'CP0 Registers', pages 70-106" is ineffective because it references a hyperlink as the location of the incorporated document.

24. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code (See Page 18 Paragraph 0041). Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Information Disclosure Statement

25. The information disclosure statement (IDS) submitted on 30 September 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. Cited Application Number 09/561,510 to Galinas et al. has not been considered, as it is unclear as to what document applicant is referring to. US Patent Number 6,778,506, which issued from

Application Number 09/561,510, does not identify Galinas as an inventor. For completeness of the record, the Examiner is citing the following documents, which are published copies of the cited application numbers: US Patent Application Publication Number 2002/0018486 (09/927,129); US Patent Number 6,778,506 (09/561,510); and US Patent Number 7,020,879 (09/312,302).

Response to Arguments

26. Applicant's arguments, see Pages 9-16, filed 19 March 2006, with respect to the rejection(s) of Claim(s) 1-7, 9-27, and 29-32 under 35 USC §§ 102, 103, and 112 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as applied above.

Conclusion

27. This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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